AMENDMENTS TO THE SPECIFICATION:

Page 4, amend the paragraph beginning at line 4 as follows:

To address this problem, a subsequent arrangement of address generator 150 split the adder and shift functions into two different logic units 160, 170, as illustrated by ~~Figure 4~~Figures 4A and 4B.

Page 5, amend the paragraph beginning at line 1 as follows:

Accordingly, the time taken to process shift instructions remains unchanged in comparison with the arrangement in ~~Figure 4~~Figures 4A and 4B since these instructions are still routed through both the shift and adder logic units 160, 170. However, the time taken by the address generator 180 to process non-shift instructions is significantly reduced in comparison with the prior arrangements since these instructions need not be routed through the shift logic unit 160, which takes additional clock cycles, but may instead by processed directly by the adder logic unit 170. It will be appreciated that such an approach can increase the overall performance of the processor core 10 when shift operations occur infrequently.

Page 13, amend the paragraph beginning at line 10 as follows:

~~Figure 4 illustrates~~Figures 4A and 4B illustrate a subsequent prior art arrangement of one stage in the pipelined processor;